Remarks

Applicant respectfully requests reconsideration of this application as amended. The specification has been amended to correct a minor informality. Claims 1, 7, 9, 10, 12, 24, and 27 have been amended. Claims 28-38 have been added. No claims have been cancelled. Therefore, claims 1, 7, 9, 10, 21, 23, 24, 26, 27, and 28-38 are presented for examination.

35 U.S.C. §101 Rejection

Claims 1, 7, 9 and 10 stand rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Claims 1, 7, 9, and 10 have been amended to recite a "computer-implemented method." As such, these claims are tied to a technological art and machine providing a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter. Therefore, applicant respectfully requests the withdrawal of the 35 U.S.C. §101 rejection.

35 U.S.C. §102(e) Rejection

Claims 21, 23, 24 and 26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Talcott (U.S. Patent No. 6,272,623). Applicant submits that the present claims are patentable over Talcott.

Talcott discloses a branch prediction scheme to predict whether a computer instruction will cause a branch to a non-sequential instruction. A prediction counter is selected by performing an exclusive OR (XOR) operation between bits from an instruction address and a hybrid history. The hybrid history, in turn, is derived by concatenating bits from a global history register with bits from a local branch history table. The bits from the

local branch history table are accessed by using bits from the instruction address. (Talcott at Abstract.)

Claim 21 recites:

> A circuit, comprising:
> a register to store a base index of a base element;
> a data shifting circuit having an input coupled to an output of the register, the data shifting circuit to shift the base index to create a shifted base index;
> an exclusive OR circuit having a first input coupled to an output of the data shifting circuit;
> multi-element array including data shift information and transform data, said array coupled to a second input of the exclusive OR circuit to transfer the transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer the data shift information to the data shifting circuit, wherein the transform data is a result of an operation performed on parameters associated the base element and all elements between the base element and an element to be predicted; and
> a prediction logic circuit coupled to an output of the exclusive OR circuit;
> wherein the exclusive OR circuit performs an exclusive OR operation on the shifted base index and the transform data to output to the prediction logic circuit a prediction index for the element to be predicted.

Applicant submits that Talcott does not disclose or suggest wherein the exclusive OR circuit performs an exclusive OR operation on the shifted base index and the transform data to output to the prediction logic circuit a prediction index for the element to be predicted, as recited by claim 21. As further recited in claim 21, the transform data is a result of an operation performed on parameters associated the base element and all elements between the base element and an element to be predicted. In light of these features, applicant can find no disclosure or suggestion of such features anywhere in Talcott. Therefore, claim 21 and its dependent claims are patentable over Talcott.

Claim 24 also recites, in part, wherein the exclusive OR circuit performs an exclusive OR operation on the shifted base index and the transform to output to the prediction logic

circuit a prediction index for an element to be predicted. As discussed above, Talcott does not disclose or suggest such a feature. Therefore, claim 24 and its dependent claims are patentable over Talcott for the reasons discussed above with respect to claim 21.

35 U.S.C. §102(b) Rejection

Claims 1, 9, 10, and 27 stand rejected under 35 U.S.C. §102(e) as being anticipated by Pan et al. (U.S. Patent No. 5,553,253). Applicant submits that the present claims are patentable over Pan.

Pan discloses a method and apparatus for predicting the outcome of branch instructions subject to execution in a multiple processor digital computer. Branch prediction is based upon a correlation between a history of successive prior branches and a specified branch instruction. A branch prediction table is also used. The fields in the table are derived and thereafter updated based upon the correlated combination of outcomes from prior branches and the branch address under consideration. (Pan at Abstract.)

Claim 1 recites:

> A computer-implemented method, comprising:
> providing at least three elements, including a first element and a last element, each element having an associated parameter;
> providing a first identifier for the first element;
> for a first sequential execution of the at least three elements, performing a first operation on the associated parameters of the at least three elements to produce a transform;
> saving the transform;
> for a second sequential execution of the elements, performing a second operation on the first identifier and the transform to produce a last identifier associated with the last element;
> using the last identifier to access a location in a multi-element prediction array including at least a shift value and a transform; and
> using a content of said location to predict a decision status of the last element.

Applicant submits that Pan does not disclose or suggest performing a first operation on the associated parameters of the at least three elements to produce a transform or performing a second operation on the first identifier and the transform to produce a last identifier associated with the last element, as recited by claim 1. First, Pan does not disclose or suggest performing a first operation on the associated parameters of the at least three elements to produce a transform. The Office Action identifies an element as being a branch instruction (i.e., A0 through A31). (Office Action mailed 9/12/05 at pg. 5, point 13a.) It further identifies A27, A28, and A29 as being the same as the parameters of the present invention. (Id.) If that is the case, then Pan does not disclose or suggest performing a first operation on the associated parameters of at least three elements. Applicant can find nowhere in Pan of bringing together at least three sets of the bits A29 through A29 per element and performing an operation on these sets.

Second, Pan does not disclose or suggest performing a second operation on the first identifier and the transform to produce a last identifier associated with the last element. The Office Action states that "[w]hen the last element, or the third branch, is taken, the 2-bit up/down counter increments the transform to produce a last identifier associated with the last element." (Id. at pg. 6, point 13e.) However, Pan does not disclose or suggest performing on operation on the ***first identifier*** and transform to produce a last identifier associated with a last element. Therefore, for all of these reasons, claim 1 and its dependent claims are patentable over Pan.

Claim 27 also recites, in part, performing a first operation on the associated parameters of the at least three elements to produce a transform and performing a second operation on the first identifier and the transform to produce a last identifier associated with

the last element. As discussed above, Pan does not disclose or suggest such a feature. Therefore, claim 27 and its dependent claims are patentable over Pan for the reasons discussed above with respect to claim 1.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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